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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,587	01/28/2004	Miwa Wake	S004-4839 (DIV)	3839

7590 03/10/2006

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/766,587	WAKE ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 4-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohsawa (U.S. 2002/0051378).

As to claim 4, Ohsawa discloses in figure 49 a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (having n-type and p-type regions as shown in figure 49) provided on a first conductivity type supporting substrate (10) through an embedded insulating film ("silicon oxide film" 11), comprising: a second conductivity type source region (having p-type in source region as shown in figure 49) and a second conductivity type drain region (having p-type in drain region as shown in figure 49) formed in the semiconductor film; a gate insulating film (16) formed on an upper surface of the semiconductor film; and a gate electrode (13) formed on an upper surface of the gate insulating film (16), wherein the source region (14a, 14b) includes an ultra-shallow high-density N-type source region (14b) at a boundary with a channel region, a low-density N-type source region (14a) under the ultra-shallow high-density N-type source region (14b), and an embedded insulating (11) neighboring N-type source region; and wherein the drain region includes an ultra-shallow high-density N-type drain region (14b) at a boundary with the channel region, a low-

density N-type drain region (14a) under the ultra-shallow high-density N-type drain region (14b), and an embedded insulating (11) neighboring N-type drain region (15a, 15b).

As to claim 5, Ohsawa discloses in figure 49 a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (having n-type and p-type regions as shown in figure 49) provided on a first conductivity type supporting substrate (10) through an embedded insulating film ("silicon oxide film" 11), further comprising: a first sidewall (element 17 on the left side of electrode 13) disposed around the gate electrode (13) and a second sidewall (element 17 on the right side of electrode 13) disposed on the first sidewall.

As to claim 6, Ohsawa discloses in figure 40 a semiconductor integrated circuit in which a CMOS transistor is formed on a first conductivity type semiconductor film (having p-type regions as shown in figure 40) provided on a first conductivity type supporting substrate (10) through an embedded insulating film ("silicon oxide film" 11), comprising: a second conductivity type source region (comprising elements 14 and 15) and a second conductivity type drain region (14, 15) formed in the semiconductor film (11); a gate insulating film ("gate oxide film" 16) formed on an upper surface of the semiconductor film (11); and a gate electrode (13) formed on an upper surface of the gate insulating film (16), wherein a channel region (comprising regions 12a, 12b) disposed under the gate insulating film (16) has a first conductivity type impurity region (12b) having a higher density ("concentration") than a well (12a) at a boundary with the drain region (region of 15) [region 12b has a high density (concentration), but region 12a has a low concentration (low density)] (see paragraph [0289]).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 2 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,713,325. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitations of "***forming a gate oxide film of a second conductivity type transistor ... providing resist as a mask on a part of the source region and the drain region adjacent to the gate electrode, and further performing ion implantation so as to form a second conductivity type impurity region in each of the source region and the drain region***" as recited in claim 2 of the instant invention have the same/identical/similar function/purpose as the limitations of "***forming a gate oxide film of a first conductivity type transistor ... forming an insulating film on the source region, the drain region, and the gate electrode ... and performing ion implantation using the sidewall as***

a mask so as to form a second conductivity type impurity region in each of the source region and the drain region" as recited in claim 1 of the U.S. Patent No. 6,713,325.

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4. Claim 3 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,713,325 in view of Ohsawa (U.S. 2002/0051378).

As to claim 3, the U.S. Patent No. 6,713,325 discloses all limitations in the claim except for the step of: forming a first conductivity type impurity region having a higher density than that of the first conductivity type impurity region in a middle depth portion of the semiconductor film serving as the proximal region to a drain in the first conductivity type impurity region.

Ohsawa discloses in figure 40 a semiconductor integrated circuit comprising the step of: forming a first conductivity type impurity region (12b) having a higher density than that of the first conductivity type impurity region (12a) in a middle depth portion of the semiconductor film serving as the proximal region to a drain (15) in the first conductivity type impurity region [region 12b has a high density (concentration), but region 12a has a low concentration (low density)] (see paragraph [0289]).

Response to Arguments

Applicant's arguments with respect to claim 6 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
3 March 2006